# Towards Side-Channel Protected X25519 on 32-bit ARM Cortex-M4 Embedded Processors

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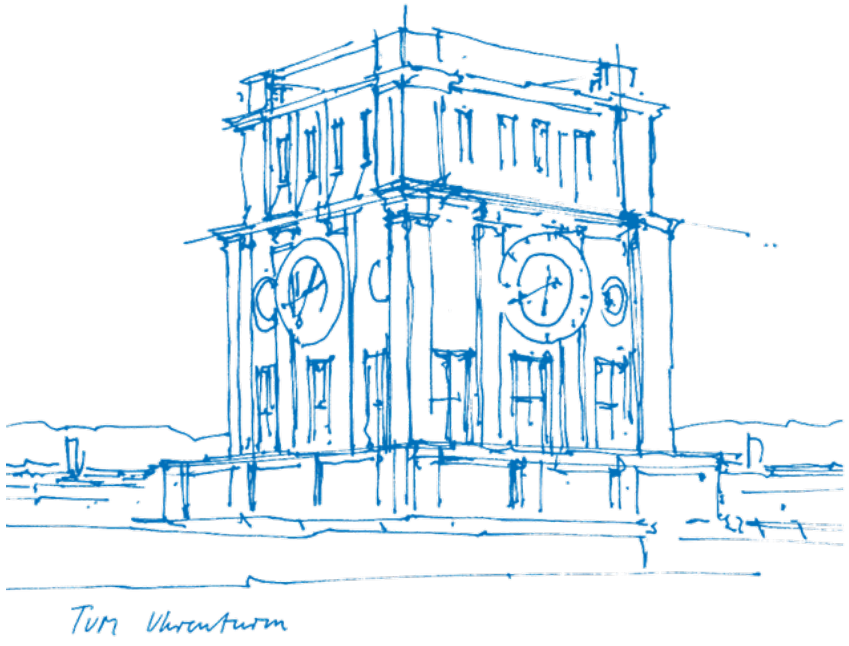

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- cf. https://safecurves.cr.yp.to/

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Montgomery curves:

$$\mathcal{M}/\mathbb{F}_p := \{(x, y) \in \mathbb{F}_p^2 \ : \ By^2 \equiv x^3 + Ax^2 + x \pmod{p}\}$$

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*Hybrid Post-Quantum Handshake X25519+NewHope:

- Boring SSL under the name CECPQ1 (Google Chrome Canary)
- Tor proposal under the name RebelAlliance

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Scalar multiplication: $\mathbf{Q} = [k] \cdot \mathbf{P} = \mathbf{P} + \mathbf{P} + \cdots + \mathbf{P}$ in the group $(\mathcal{M}/\mathbb{F}_p \cup \mathcal{O}, +)$.

# Montgomery Ladder Algorithm

**Input:** $k = (k_{m-1}, \ldots, k_0)_2 \in \mathbb{N}$, $\mathbf{P} \in \mathcal{M}/\mathbb{F}_p$
**Output:** $\mathbf{Q} = [k] \cdot \mathbf{P} \in \mathcal{M}/\mathbb{F}_p$
$\mathbf{R}_0 \leftarrow \mathcal{O}$; $\mathbf{R}_1 \leftarrow \mathbf{P}$
**for** $i \leftarrow (m-1)$ **downto** 0 **do**
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- X25519 in $1287\mathbf{M} + 1274\mathbf{S} + 2040\mathbf{A} + 255\mathbf{M}_{121666}$ when inversion in $\mathbb{F}_p$ takes $254\mathbf{S} + 11\mathbf{M}$.

# ARM Cortex M4 Processors

- ARMv7E-M architecture
- 32-bit Thumb®-2 instruction set
- 3-stage pipeline
- $13 + 1$ General-purpose registers
- Optional FPU Unit
- DSP Unit ($32 \times 32$-bit Multiplier :-)

- 32-bit STM32F411RE MCU
- 100 MHz ARM Cortex-M4F
- 512-kB Flash
- 128-kB SRAM
- $I_0 = 100\mu$A/MHz

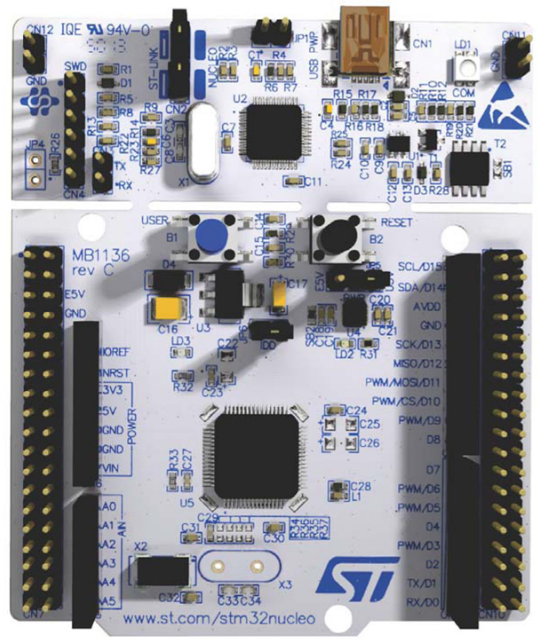


Figure : STMicroelectronics NUCLEO-F411RE

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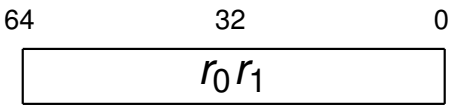

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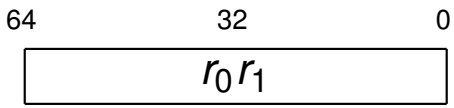


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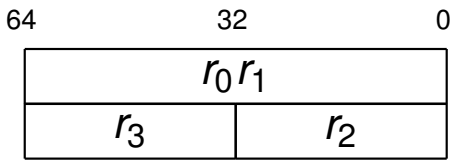

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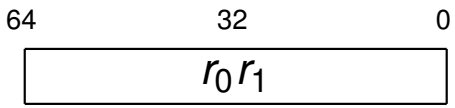


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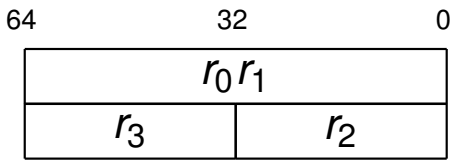


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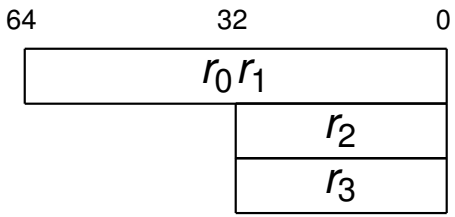
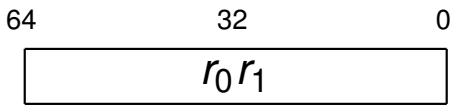


# ARM Cortex M4 Instructions

Powerful DSP instructions:

- `UMULL` $r_2, r_3, r_0, r_1$:
  $r_2 + r_3 2^{32} = r_0 r_1$

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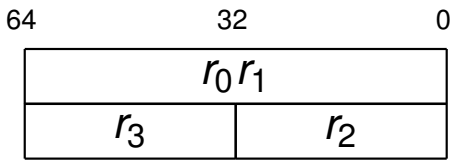


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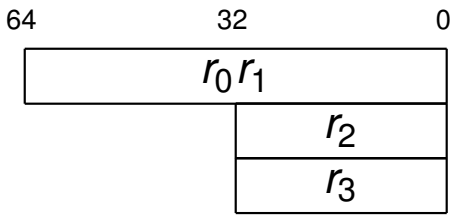


No carry flags.

# Representation of Integer Numbers and Modular Reduction

- 255-bit integers are represented in radix-$2^{32}$ using 8-limbs:

$$(a_0, \ldots, a_7) \Longleftrightarrow a = \sum_{i=0}^{7} a_i 2^{32i},\ a_i \in \mathbb{Z}_{2^{32}}$$

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  - Fit values into 256-bit
  - Aligned to the registers boundaries

- Full reduction modulo $p = 2^{255} - 19$ at the very end
  - Fit back values to the original field $\mathbb{F}_p$

# Modular Addition/Substraction

1. Straightforward addition with carry (8 `AD?S` instructions):

   **Input:** $a = (a_0, \ldots, a_7)$, $b = (b_0, \ldots, b_7)$.
   **Output:** $c = a + b = (c_0, \ldots, c_7, \gamma_8)$
   $\gamma_0 \leftarrow 0$
   **for** $i \leftarrow 0$ **to** 7 **do**
   $(c_i, \gamma_{i+1}) \leftarrow a_i + b_i + \gamma_i$
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Total: 106 cycles in 138 bytes.

# $256 \times 256$-bit Multiplication/Squaring

Subtractive Karatsuba:

$$\begin{aligned} ab &= (a_0 + a_1 2^{n/2})(b_0 + b_1 2^{n/2}) \\ &= a_0 b_0 + [(-1)^{(1-t)} |a_0 - a_1||b_0 - b_1| + a_1 b_1 + a_0 b_0] 2^{n/2} + a_1 b_1 2^n \end{aligned}$$

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Costs:

- 3 multiplications
- 2 additions + 2 subtractions + some shifting
- 2 absolute differences and 1 conditional negation

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Costs:

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- 2 additions + 2 subtractions + some shifting
- 2 absolute differences and 1 conditional negation

First option:

- 3-level subtractive Karatsuba $\Longrightarrow$ $27\times$ $(32 \times 32)$-bit multiplications

Second option:

- 2-level subtractive Karatsuba $\Longrightarrow$ $9\times$ $(64 \times 64)$-bit multiplications ✓

Total: 546 cycles and $1,264$ bytes.

# $64 \times 64$-bit Multiplication/Squaring

$$(a_0 + a_1 2^{32})(b_0 + b_1 2^{32}) = a_0 b_0 + (a_0 b_1 + a_1 b_0)2^{32} + a_1 b_1 2^{64}$$

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Partial Products (4 × `UMULL`):

$$(d_0, d_1) = a_0 b_0$$
$$(d_2, d_3) = a_0 b_1$$
$$(d_4, d_5) = a_1 b_0$$
$$(d_6, d_7) = a_1 b_1$$

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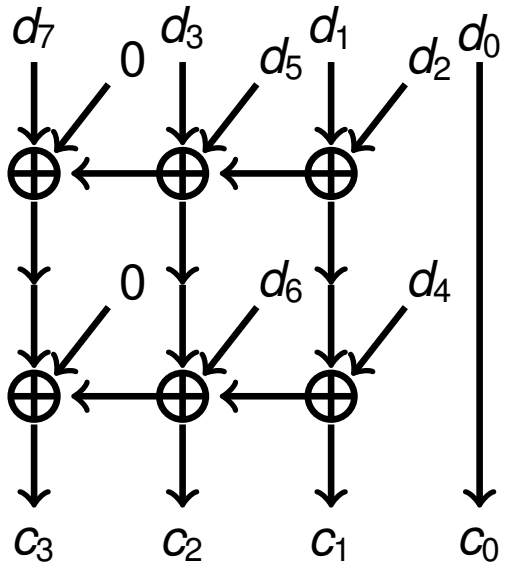
Adder Tree (2 × `ADDS` + 2 × `ADCS` + 2 × `ADC`):



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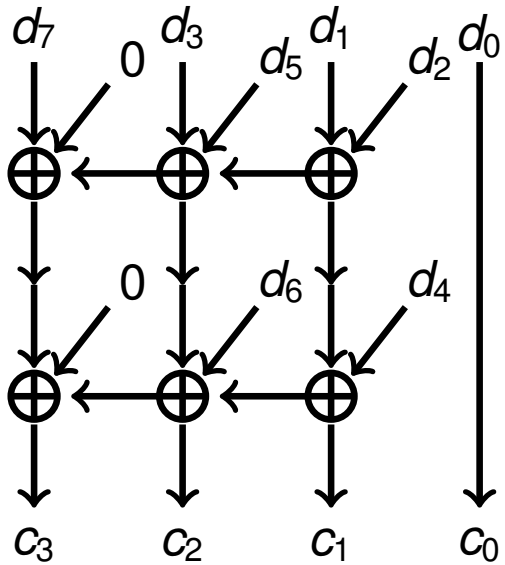


Total: 10 instructions.

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$c_0 \leftarrow 0$
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    $(c_i, c_{i+1}) \leftarrow 121666 a_i + c_i$
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$121665a_i + c_i + a_i$ ✓

In total: $1\texttt{UMULL} + 7\texttt{UMAAL} + 1\texttt{SUB} = 9$ instructions.

# Implementation Results

$\mathbb{Z}_{2p}$ Arithmetic

| Operation | Speed [Cycles] | Code [Bytes] | Stack [Bytes] |
|---|---|---|---|
| Addition | 106 | 138 | 32 |
| Subtraction | 108 | 148 | 32 |

- GNU Compiler Collection for ARM Embedded Processors version `4.9.3` with `-O2 -mthumb -mcpu=cortex-m4`
- Incl. reduction modulo $2p$ and function call overheads.

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| Inversion (254S+11M) | 96,337 | 484 | 480 |

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# Implementation Results

Variable-base Single-scalar Multiplication

| | Platform | 256 × 256-bit Multiply [Cycles] | 256-bit Square [Cycles] | S/M Ratio | Curve25519 [Cycles] | Curve25519 [Bytes] |
|---|---|---|---|---|---|---|
| 8-bit | AVR ATmega [1] | 6,868 | – | 1 | 22,791,580 | – |
| | AVR ATmega [2] | 7,555 | 5,666 | 0.75 | 20,153,658 | – |
| | AVR ATmega [3] | 4,961 | 3,324 | 0.67 | 13,900,397 | 17,710 |

[1] M. Hutter and P. Schwabe “NaCl on 8-Bit AVR Microcontrollers”, AFRICACRYPT 2013.
[2] E. Nascimento et al. “Efficient and Secure Elliptic Curve Cryptography for 8-bit AVR Microcontrollers”, SPACE 2015.
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| 16-bit | MSP430 [4] | 3,606 | – | 1 | 9,139,739 | 11,778 |
| | MSP430 [3] | 3,193 | 2,426 | 0.76 | 7,933,296 | 13,112 |
| | MSP430 [4] | 2,488 | – | 1 | 6,513,011 | 8,956 |
| | MSP430 [3] | 2,079 | 1,563 | 0.75 | 5,301,792 | 10,088 |


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| 32-bit | ARM Cortex-M0 [3] | 1,294 | 857 | 0.66 | 3,589,850 | 7,900 |
| | ARM Cortex-M4 [5] | 631 | 563 | 0.89 | 1,816,351 | 4,140 |
| | **ARM Cortex-M4 [This Work]** | 546 | – | 1 | **1,658,083** | **2,952** |
| | **ARM Cortex-M4 [This Work]** | 546 | 362 | 0.66 | **1,423,667** | **3,750** |


[1] M. Hutter and P. Schwabe “NaCl on 8-Bit AVR Microcontrollers”, AFRICACRYPT 2013.
[2] E. Nascimento et al. “Efficient and Secure Elliptic Curve Cryptography for 8-bit AVR Microcontrollers”, SPACE 2015.
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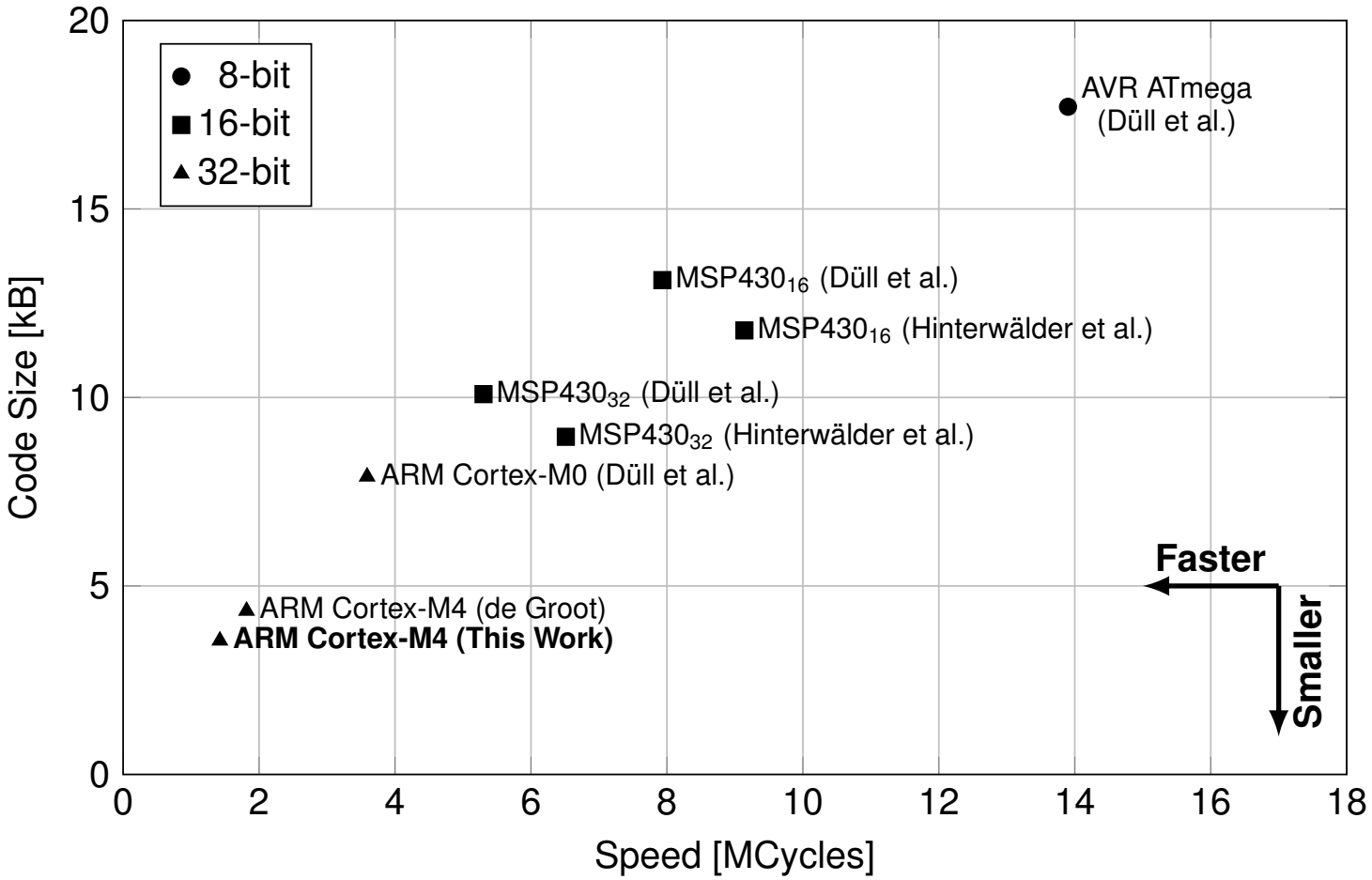
[5] W. de Groot “"A Performance Study of X25519 on Cortex M3 and M4”, Master Thesis 2015.

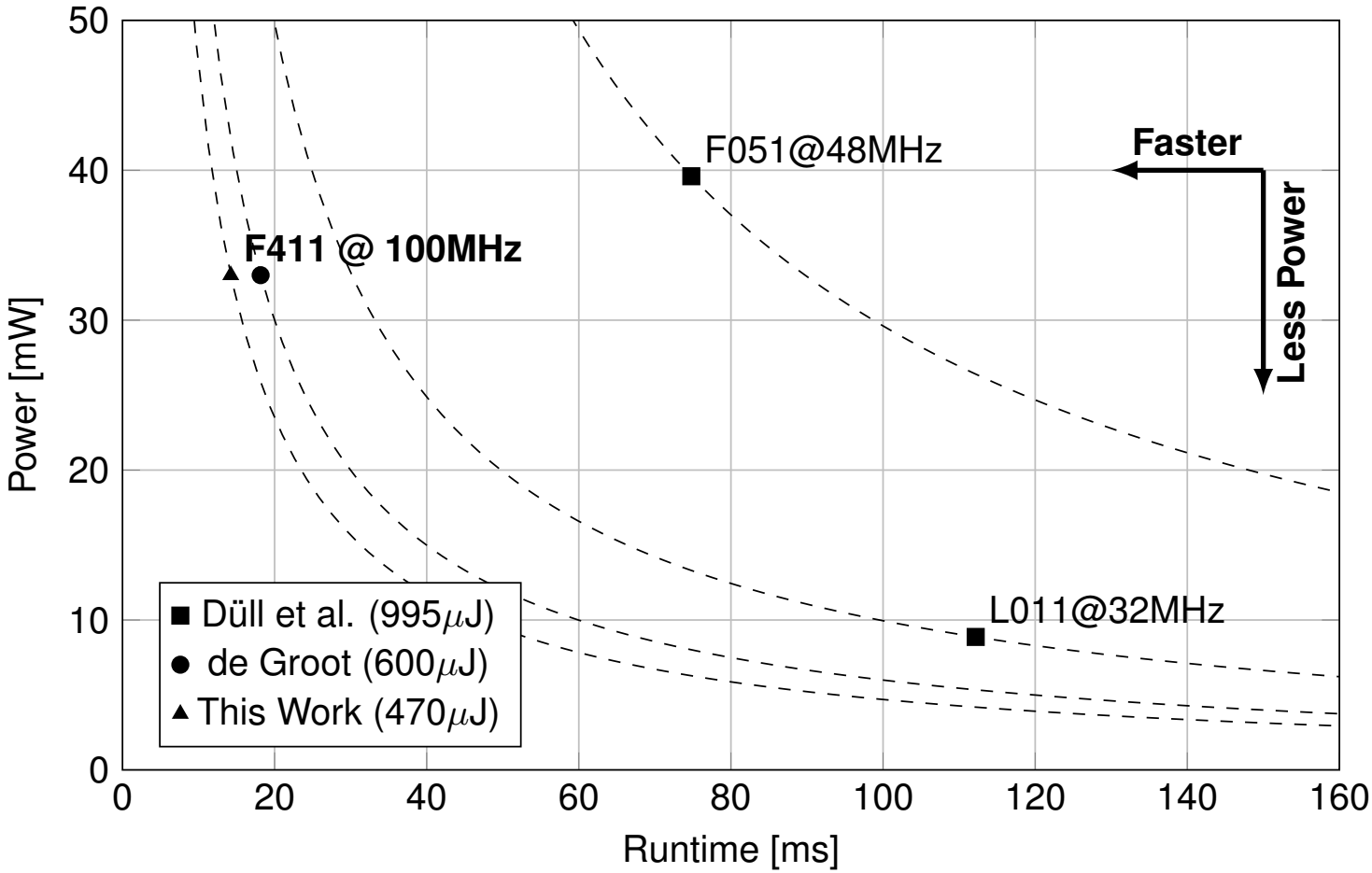
# Implementation Results

Area vs Speed



# Implementation Results

Power/Energy vs Runtime



# Adding more Side-Channel Protections to X25519

## Randomized Projective Coordinates

$x \mapsto (\lambda X, \lambda Z)$ for $\lambda \leftarrow^{\$} \mathbb{F}^*_{2^{255}-19}$

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- Incl. cycles for setting up and generating 64-bytes randomness with ChaCha20

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Is this all? cf. https://eprint.iacr.org/2016/923.pdf

# Towards Higher Security Levels

X448

Curve448 (RFC7748):

- $p = 2^{448} - 2^{224} - 1$, $B = 1$, $A = 156326$.

Preliminary results:

# Towards Higher Security Levels

X448

Curve448 (RFC7748):

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Preliminary results:

- 1-level additive Karatsuba

# Towards Higher Security Levels

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Curve448 (RFC7748):

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- X448 @ $6,939,815$ cycles $\approx$ 69ms@100MHz

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IETF/TLS cipher suite as by RFC7905 and RFC7539:

- ChaCha20-Poly1305 AEAD @ 33.6 cycles/byte in $1,668$ bytes ✓

# Conclusion

High-speed and compact X25519 on ARM Cortex M4 processors

- High-speed full-radix field arithmetic
- Exploit powerful DSP multiplication instructions
- Promising results for high-speed IoT applications

Next steps:

1. Ultimate the porting of NaCl on ARM Cortex M4 processors
2. Validate Side-Channel Protections against actual measurements
3. Evaluate various efficiency-security trade-offs, e.g. X448/Ed448